REMARKS

This responds to Office Action mailed on October 15, 2007.

Claims <u>1-3, 5-7, 11, 12, and 14-20</u> are amended, claims <u>21-30</u> are canceled, and no claims are added; as a result, claims 1-20 are now pending in this application.

Affirmation of Election

As provisionally elected by Applicants representative, Dana B. LeMoine, on October 2, 2007, Applicants elect to prosecute the invention of Group I, claims 1-20. Claims 21-30 are hereby canceled. However, Applicant reserves the right to later file continuations or divisionals having claims directed to the non-elected inventions.

35 USC § 103 Rejection of the Claims

Claims 1-20 were rejected under 35 USC § 103 (a) as being unpatentable over "A VLSI 128 - Processor Chip for Multiresolution Image Processing" to Albanesi et al. in view of U.S Patent No. 7,200,837 B2 to Stevens.

Albanesi discloses a mesh of processing elements and a mesh of switching elements. See section 2.1 "The mesh of elementary processors" and section 2.2 "The mesh of switching elements". As described in section 2.2, "[t]he configuration of the mesh of switching element is uniform throughout the chip. It is controlled by two bits (B, H/V) of the control code that selects one of the three schemes ... correspond[ing] to B-, H- and V-modes." Accordingly, the mesh of switching elements is a single interconnect mesh, and the entire mesh of switching elements is uniformly controlled by two bits of information (B, H/V). Applicants note that the term "mesh" is used in Albanesi to describe the array of processors as well as the single interconnect mesh; however, in the instant application, the term "mesh" is used only to refer to the interconnect.

In contrast to Albanesi, the apparatus described in the instant application includes two separate mesh interconnect networks. Each of the mesh interconnect networks may be allocated to data or control or a combination thereof. The independent claims have been amended to make this distinction clear. Many of the dependent claims have also been amended to maintain proper antecedent basis.

Independent claims 1, 7, and 11 have been amended to clearly recite that the plurality of heterogeneous processing elements are coupled to a plurality of routers, that the plurality of routers are interconnected by a plurality of mesh interconnect networks, and that the plurality of mesh interconnect networks are allocable to either data or control or a combination thereof.

Applicants respectfully submit that the Albanesi and Stevens references, taken alone or in combination, do not disclose, teach, or suggest these limitations.

Independent claim 15 has been amended to clearly recite first and second mesh interconnect networks in addition to the heterogeneous network of processing elements, wherein the apparatus is programmable to utilize the first and second mesh interconnect networks for any combination of data and control. Applicants respectfully submit that Albanesi only discloses one interconnect network in addition to the network of processors. Accordingly, Applicants respectfully submit that claim 15 defines over the references of record.

Regarding dependent claims 3, 5, 12, 14, and 18-20, the office action alleges that Albanesi discloses different planes for allocating control and data. Applicants respectfully submit that the claims as amended make clear that each plane can be allocated as a dedicated data plane or control plane, or can be allocated as a combination data/control plane. Applicants further submit that Albanesi does not disclose these limitations.

Reservation of Rights

Applicants do not admit that references cited under 35 USC §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserve the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Page 8 Dkt: 80107.118US1

Serial Number: 10/789,187 Filing Date: February 27, 2004

Title: ALLOCATION OF COMBINED OR SEPARATE DATA AND CONTROL PLANES

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney (952-473-8800) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-4238

Respectfully submitted,

HOOMAN HONARY ET AL.

By their Representatives,

Customer Number: 45445

Telephone Number: 952-473-8800

Date 1-15-08

Dana B. LeMoine Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail S bp Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of January, 2008.

Name